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Estimating Power Dissipation for ADSP-21368 SHARC® Processors

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Introduction

This EE-Note discusses power consumption of ADSP-21367, ADSP-21368, and ADSP-21369 SHARC® processors (hereafter referred to as ADSP-21368 processors) based on characterization data measured over power supply voltage, core frequency (CCLK), and junction temperature (T_J). The intent of this document is to assist board designers in estimating their power budget for power supply design and thermal relief designs using ADSP-21368 processors.

ADSP-21368 processors are members of the SIMD SHARC family of processors, featuring Analog Devices Super Harvard Architecture. Like other SHARC processors, the ADSP-21368 is a 32-bit processor optimized for high-precision signal processing applications.

ADSP-21368 processors are offered in the commercial and industrial temperature ranges at core clock frequencies of 266-333 and 400 MHz. The 266-333 MHz processors operate at a core voltage of 1.2 V (V_{DDINT}), and the 400 MHz processors operate at a core voltage of 1.3 V (V_{DDINT}). The I/O of all ADSP-21368 processors operates at 3.3 V (V_{DDEXT}).

The total power consumption of the ADSP-21368 processor is the sum of the power consumed for each of the power supply domains (V_{DDINT}, V_{DDEXT}, and A_{VDD}). The total power consumption has two components: one due to internal circuitry (i.e., the core and the PLL), and the other due to the switching of external output drivers (i.e., the I/O). The following sections detail how to derive both of these components for estimating total power consumption based on different dynamic activity levels, I/O activity, power supply settings, core frequencies, and environmental conditions.

Estimating Internal Power Consumption

The total power consumption due to internal circuitry (on the V_{DDINT} supply) is the sum of the static power component and dynamic power component of the processor's core logic. The dynamic portion of the internal power is dependent on the instruction execution sequence, the data operands involved, and the instruction rate. The static portion of the internal power is a function of temperature and voltage; it is not related to processor activity.

Analog Devices provides current consumption figures and scaling factors for discrete dynamic activity levels. System application code can be mapped to these discrete numbers to estimate the dynamic portion of the internal power consumption for an ADSP-21368 processor in a given application.

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Internal Power Vector Definitions and Activity Levels

The following power vector definitions define the dynamic activity levels that apply to the internal power vectors shown in Table 1.

- $I_{DD\text{-}IDLE}$ V_{DDINT} supply current for idle activity. Idle activity is the core executing the `IDLE` instruction only, with no core memory accesses, no DMA, and no interrupts.
- $I_{DD\text{-}INLOW}$ V_{DDINT} supply current for low activity. Low activity is the core executing a single-function instruction fetched from internal memory, with no core memory accesses, no DMA, and no activity on the external port.
- $I_{DD\text{-}INMED}$ V_{DDINT} supply current for medium activity. Medium activity is the core executing a multi-function instruction fetched from internal memory and a `NOP`, with 8 core memory accesses per `CLKIN` cycle (DMx64), DMA through three SPORTs running at 3.47 MHz, and no SDRAM or AMI activity on the external port. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random.
- $I_{DD\text{-}INHIGH}$ V_{DDINT} supply current for high activity. High activity is the core executing a multi-function instruction fetched from internal memory, with 16 core memory accesses per `CLKIN` cycle (DMx64) and DMA through three SPORTs running at 3.47 MHz, and no SDRAM or AMI activity on the external port. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random.
- $I_{DD\text{-}INPEAK}$ V_{DDINT} supply current for peak activity. Peak activity is the core executing a multi-function instruction fetched from internal memory and/or cache, with 32 core memory accesses per `CLKIN` cycle (DMx64, PMx64), DMA through six SPORTs running at 41.67 MHz, and no SDRAM or AMI activity on the external port. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random.

  The test code used to measure $I_{DD\text{-}INPEAK}$ represents worst-case processor operation. This activity level is not sustainable under normal application conditions.

- $I_{DD\text{-}INPEAK\text{-}TYP}$ V_{DDINT} supply current for *typical* peak activity. *Typical* peak activity is the core executing a multi-function instruction fetched from internal memory and/or cache, with 32 core memory accesses per `CLKIN` cycle (DMx64, PMx64), DMA through six SPORTs running at 41.67 MHz, DMA through one SPI running at 833 KHz, and SDRAM accesses through the external port running at 166 MHz. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access, DMA and SDRAM access is random. The SDRAM accesses are split between 60% reads and 40% writes.

Table 1 summarizes the low, medium, high, peak, and *typical* peak dynamic activity levels corresponding to the internal power vectors listed above and in Table 2.

Operation	Low	Medium	High	Peak	Peak (Typical)
Instruction Type	Single-function	Multi-function	Multi-function	Multi-function	Multi-function
Instruction Fetch	Int Memory	Int Memory, NOP	Int Memory	Int Memory, Cache	Int Memory, Cache
Core Memory Access [1]	None	8 per tCK cycle [2]	16 per tCK cycle [2]	32 per tCK cycle [3]	32 per tCK cycle [3]
DMA Transmit Int to Ext Ext Port SDRAM SPORTs SPI	 SDCLK only N/A N/A	 SDCLK only 3 @ 1/96*CCLK N/A	 SDCLK only 3 @ 1/96*CCLK N/A	 SDCLK only 6 @ 1/8*CCLK N/A	 60/40 RD/WR 6 @ 1/8*CCLK N/A
Data Bit Pattern for Core Memory Access and DMA	N/A	Random	Random	Random	Random
Ratio – Continuous Instruction Loop to SDRAM Control Code	100% Instruct Loop	100% Instruction Loop	100% Instruction Loop	100% Instruction Loop	50::50 60::40 70::30

Table 1. Dynamic activity level definitions

Estimating I_{DDINT} Dynamic Current, $I_{DD\text{-}DYN}$

Two steps are involved in estimating the dynamic power consumption due to the internal circuitry (i.e., on the V_{DDINT} supply). The first step is to determine the dynamic baseline current, and the second step is to determine the percentage of activity for each discrete power vector with respect to the entire application.

I_{DD} Baseline Dynamic Current, $I_{DD\text{-}BASELINE\text{-}DYN}$

The ADSP-21368 $I_{DD_BASELINE_DYN}$ current graph is shown in Appendix A. Note that the $I_{DD_BASELINE_DYN}$ current is derived using the $\mathbf{I_{DD\text{-}INHIGH}}$ dynamic activity level vs. core frequency. Each curve in the graph represents a baseline I_{DDINT} dynamic current for a specified power supply setting. Using the curve specific to the application, the baseline dynamic current ($I_{DD_BASELINE_DYN}$) for the V_{DDINT} power supply domain can be estimated at the operating frequency of the processor in the application. For example, with the core operating at 1.2 V (V_{DDINT}) and a frequency of 333 MHz, the corresponding baseline dynamic current ($I_{DD_BASELINE_DYN}$) for the V_{DDINT} power supply domain would be approximately 0.76 A.

I_{DD} Dynamic Current Running Your Application

Table 2 lists the scaling factor for each activity level, used to estimate the dynamic current for each specific application. With knowledge of the program flow and an estimate of the percentage of time spent at each activity level, the system developer can use the baseline dynamic current ($I_{DD_BASELINE_DYN}$) shown in Figure 4 and the corresponding activity scaling factor from Table 2 to determine the dynamic portion of the internal current ($I_{DD\text{-}DYN}$) for each ADSP-21368 processor in a system.

[1] tCK = CLKIN; Core clock ratio 16:1

[2] DMx64 accesses

[3] DMx64, PMx64 accesses

Power Vector	Activity Scaling Factor (ASF)
$I_{DD-IDLE}$	0.21
$I_{DD-INLOW}$	0.40
$I_{DD-INMED}$	0.85
$I_{DD-INHIGH}$	1.00
$I_{DD-INPEAK}$	1.13
$I_{DD-INPEAK-TYP}$ 50 :: 50 60 :: 40 70 :: 30	 0.65 0.71 0.75

Table 2. Internal power vectors and dynamic scaling factors

The dynamic current consumption for an ADSP-21368 processor in a specific application is calculated according to the following formula, where "%" is the percentage of the overall time that the application spends in that state:

(% *Peak activity level* x $I_{DD-INPEAK}$ *ASF* x $I_{DD_BASELINE_DYN}$)
(% *High activity level* x $I_{DD-INHIGH}$ *ASF* x $I_{DD_BASELINE_DYN}$)
(% *High activity level* x $I_{DD-INMED}$ *ASF* x $I_{DD_BASELINE_DYN}$)
(% *Low activity level* x $I_{DD-INLOW}$ *ASF* x $I_{DD_BASELINE_DYN}$)
+(% *Idle activity level* x $I_{DD-IDLE}$ *ASF* x $I_{DD_BASELINE_DYN}$)

= *Total Dynamic Current for* V_{DDINT} (I_{DD-DYN})

Equation 1. Internal dynamic current (I_{DD-DYN})

For example, after profiling the application code for a particular system, activity is determined to be proportioned as follows.

(10% Peak Activity Level)
(30% High Activity Level)
(50% Med. Activity Level)
(10% Low Activity Level)
(0% Idle Activity Level)

Figure 1. Internal system activity levels

Using the activity scaling factor (*ASF*) provided for each activity level in Table 2 (and the core operating at 1.2 V (V_{DDINT}) and 333 MHz), a value for the dynamic portion of the internal current consumption of a single processor can be estimated as follows.

*(10% **x 1.13** x 0.76)*
*(30% **x 1.00** x 0.76)*
*(50% **x 0.85** x 0.76)*
*(10% **x 0.40** x 0.76)*
*+ (0% **x 0.21** x 0.76)*

I_{DD-DYN} = *0.67A*

Figure 2. Internal dynamic current estimation

Therefore, the total estimated dynamic current on the V_{DDINT} power supply in this example is 0.67 A.

Estimating I_{DDINT} Static Current, $I_{DD-STATIC}$

The ADSP-21368 $I_{DD-STATIC}$ current graphs for the MQFP and LQFP 266 MHz and 333 MHz processor speed grade models are shown in Appendix B, and the Super BGA 333 MHz and 400 MHz processor speed grade models are shown in Appendix C. The static current on the V_{DDINT} power supply domain is a function of temperature and voltage but is *not* a function of frequency or activity level. Therefore, unlike the dynamic portion of the internal current, the static current does not need to be calculated for each discrete activity level or power vector. Using the static current curve corresponding to the application (i.e., at the specific V_{DDINT}), the baseline static current ($I_{DD-STATIC}$) can be estimated vs. junction temperature (T_J) of the for estimating T_J).

For example, in an application with the core operating at 1.2V (V_{DDINT}) and the ADSP-21368 processor at a junction temperature (T_J) of +100°C, the corresponding baseline static current ($I_{DD-STATIC}$) for the V_{DDINT} power supply domain would be approximately 0.56 A.

The ADSP-21368 static power is constant for a given voltage and temperature. Therefore, it is simply added to the total estimated dynamic current when calculating the total power consumption due to the internal circuitry of the ADSP-21368 processor. Note that the $I_{DD-STATIC}$ current shown in Figure 5 represents the worst-

case static current as measured across the wafer fabrication process for the ADSP-21368 device.

Estimating Total I_{DDINT} Current

The total current consumption due to the internal core circuitry (I_{DDINT}) is the sum of the dynamic current component and the static current component as shown in Equation 2.

$$I_{DDINT} = I_{DD\text{-}DYN} + I_{DD\text{-}STATIC}$$

Equation 2. Internal core current (I_{DDINT}) calculation

Continuing with the example (the processor operating at 1.2 V and 333 MHz, and with the code as profiled), assume that the resulting junction temperature (T_J) is estimated to be +100°C. The total internal current consumed by the processor core under these conditions would then be:

$$I_{DDINT} = 0.67 + 0.56 = 1.23A$$

Equation 3. Total internal core current estimation

Each ADSP-21368 processor includes an analog phase-lock loop (PLL) and related internal circuitry to provide clock signals to the core and peripheral logic. This circuitry receives power through the A_{VDD} power supply pin of the processor. Compared to the processor core, this circuitry consumes little power. However, since it is always active, it should be considered when calculating the overall power consumed by the internal circuitry of each ADSP-21368 processor.

The ADSP-21368 data sheet indicates that the maximum A_{IDD} per processor is 10 mA; therefore, the total expected internal current consumed by the processor core and the PLL logic under the conditions described in the example would be:

$$I_{DDINT} = 0.67 + 0.56 + 0.01 = 1.24A$$

Equation 4. Total internal current estimation

Total Estimated Internal Power, P_{DDINT}

The resulting internal power consumption (P_{DDINT}) is given by Equation 5.

$$P_{DDINT} = V_{DDINT} \text{ x } I_{DDINT}$$

Equation 5. Internal power (P_{DDINT}) calculation

Using Equation 5, the total estimated internal power consumed by the processor in the application described in this example would be:

$$P_{DDINT} = 1.2V \text{ x } 1.24A = 1.49W$$

Equation 6. Total internal power (P_{DDINT}) estimation

Estimating External Power Consumption

The external power consumption (on the V_{DDEXT} supply) is dependent on the switching of the output pins. The magnitude of the external power depends on:

- The number of output pins that switch during each cycle, *O*
- The maximum frequency at which the output pins can switch, *f*
- The voltage swing of the output pins, V_{DDEXT}
- The load capacitance of the output pins, C_L

In addition to the input capacitance of each device connected to an output, the total load capacitance should include the capacitance (C_{OUT}) of the processor pin itself, which is driving the load.

The SDRAM controller is capable of running up to 166 MHz and can run at various frequencies, depending on the programmed SDRAM clock (`SDCLK`) to core clock (`CCLK`) ratio. The maximum read/write throughput of the asynchronous memory interface (AMI) is one 32-bit word per 3 `SDCLK` cycles (wait state of 2). This corresponds to a maximum switching frequency of 83.3 MHz for `ADDR23-0` and

DATA31-0 during SDRAM writes and a maximum switching frequency of 27.8 MHz for ADDR23-0 and DATA31-0 during writes to external asynchronous memories.

In addition, the serial ports (SPORTs) and serial peripheral interface (SPI) can operate up to one-eighth (1/8) the processor core clock rate (CCLK). With a core clock of 333 MHz, this corresponds to a maximum switching frequency of 20.8 MHz for SDATA and MOSI/MISO, and maximum switching frequency of 41.7 MHz for SCLK and SPICLK.

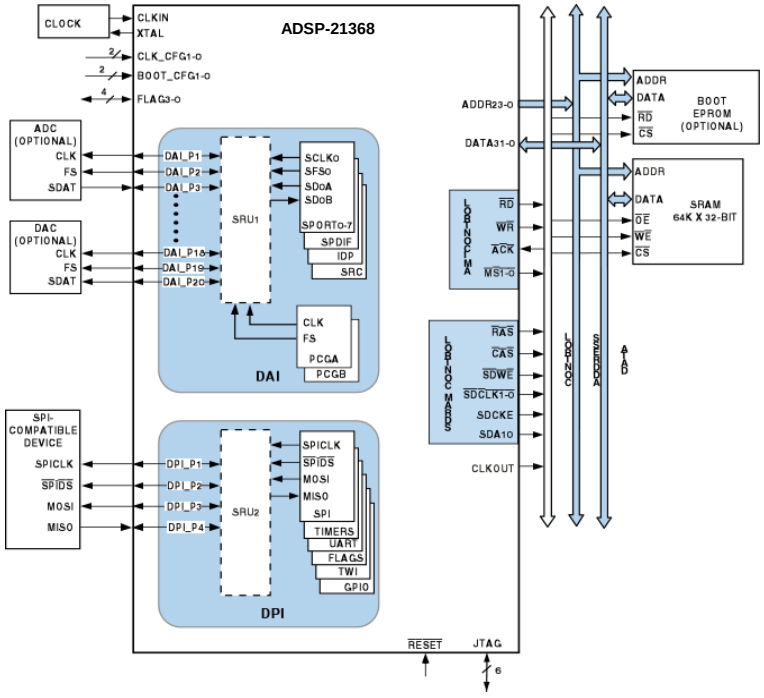

Figure 3. ADSP-21368 system sample configuration

Equation 7 shows how to calculate the average external current (I_{DDEXT}) using the above parameters:

$$I_{DDEXT} = O \ x \ f \ x \ V_{DDEXT} \ x \ C_L$$

Equation 7. External current (I_{DDEXT}) calculation

The estimated average external power consumption (P_{DDEXT}) can be calculated as follows:

$$P_{DDEXT} = V_{DDEXT} \ x \ I_{DDEXT}$$

Equation 8. External power (P_{DDEXT}) calculation

Using the sample configuration (Figure 3), we can estimate the external current and thereby the external power consumption with the following assumptions:

- Processor core running at 333 MHz (CCLK)
- 64K x 32 bit external SRAM, C_L = 10 pF (trace capacitance ignored)
- Writes to external memory occur with WS =2
- During external memory writes, 50% of the ADDR23-0 and DATA31-0 pins are switching
- DAI configured as SPORT transmitting and receiving 32-bit words at 1/8*CCLK, C_L = 10 pF (trace capacitance ignored)
- DPI configured as SPI transmitting and receiving 32-bit words at 1/8*CCLK, C_L = 10 pF (trace capacitance ignored)
- Output capacitance of processor pin, C_{OUT} = 4.7 pF

The external current (I_{DDEXT}) (Equation 6) can be calculated for each class of pins that can drive and is shown in Table 3.

Summing the individual currents from Table 3, the total external current (I_{DDEXT}) for the sample configuration shown in Figure 3 would be 0.077 A.

Using this current, the estimated average external power is calculated as:

$$P_{DDEXT} = 3.3V \times 0.077A = 0.254W$$

Equation 9. External power (P_{DDEXT}) calculation for sample configuration shown in Figure 3

Pin Type	No. of Pins	% Switching	x f	x V_{DDEXT}	x C	I_{DDEXT}
ADDR[23:0]	24	50	27.8 MHz	3.3V	4.7pF + (2 x 10pF)	0.02719
DATA[31:0]	32	50	27.8 MHz	3.3V	4.7pF + (2 x 10pF)	0.03626
$\overline{RD}$	1	0	n/a	3.3V	4.7pF + (2 x 10pF)	0.00000
$\overline{WR}$	1	100	55.6 MHz	3.3V	4.7pF + (1 x 10pF)	0.00270
MS[1:0]	1	0	n/a	3.3V	4.7pF + (1 x 10pF)	0.00000
SDCLK[0]	1	100	166 MHz	3.3V	4.7pF + (0 x 10pF)	0.00257
DAI_P1 (SCLK)	1	100	41.7 MHz	3.3V	4.7pF + (1 x 10pF)	0.00202
DAI_P2 (FS)	1	100	1.3 MHz	3.3V	4.7pF + (1 x 10pF)	0.00006
DAI_P3 (SDATA)	1	0	n/a	3.3V	4.7pF + (1 x 10pF)	0.00000
DAI_P18 (SCLK)	1	100	41.7 MHz	3.3V	4.7pF + (1 x 10pF)	0.00202
DAI_P19 (FS)	1	100	1.3 MHz	3.3V	4.7pF + (1 x 10pF)	0.00006
DAI_P20 (SDATA)	1	100	20.8 MHz	3.3V	4.7pF + (1 x 10pF)	0.00101
DPI_P1 (SPICLK)	1	100	41.7 MHz	3.3V	4.7pF + (1 x 10pF)	0.00202
DPI_P2 (SPIDS)	1	0	n/a	3.3V	4.7pF + (1 x 10pF)	0.00000
DPI_P3 (MOSI)	1	100	20.8 MHz	3.3V	4.7pF + (1 x 10pF)	0.00101
DPI_P4 (MISO)	1	0	n/a	3.3V	4.7pF + (1 x 10pF)	0.00000

Table 3. External current (I_{DDEXT}) summary for Figure 3.

Total Power Consumption

For a particular system, the total power consumption becomes the sum of its individual components, the power consumed by the internal circuitry, and the power consumed due to the switching of the I/O pins, as follows:

$$P_{TOTAL} = P_{DDINT} + P_{DDEXT}$$

Equation 10. Total power (P_{TOTAL}) calculation

Where: P_{DDINT} = Internal power consumption as defined by Equation 5

P_{DDEXT} = External power consumption as defined by Equation 8

For example, if we assume that the processor in Figure 3 is operating under the conditions detailed in the example (the processor operating at 1.2 V, 333 MHz, and code as profiled in Figure 1) and we also assume the resulting junction temperature (T_J) has been estimated to be +100°C (see Appendix B for estimating T_J), the total estimated power consumed would be:

$$P_{TOTAL} = 1.49W + 0.254W = 1.74W$$

Equation 11. Total power (P_{TOTAL}) calculation for sample configuration shown in Figure 2 while running code described in Example 1

Appendix A

The ADSP-21368 $I_{DD_BASELINE_DYN}$ current graph is shown in Figure 4. The $I_{DD_BASELINE_DYN}$ current is derived using the $\boldsymbol{I_{DD\text{-}INHIGH}}$ dynamic activity level vs. core frequency. Each curve in the graph represents a baseline I_{DDINT} dynamic current for a specified power supply setting.

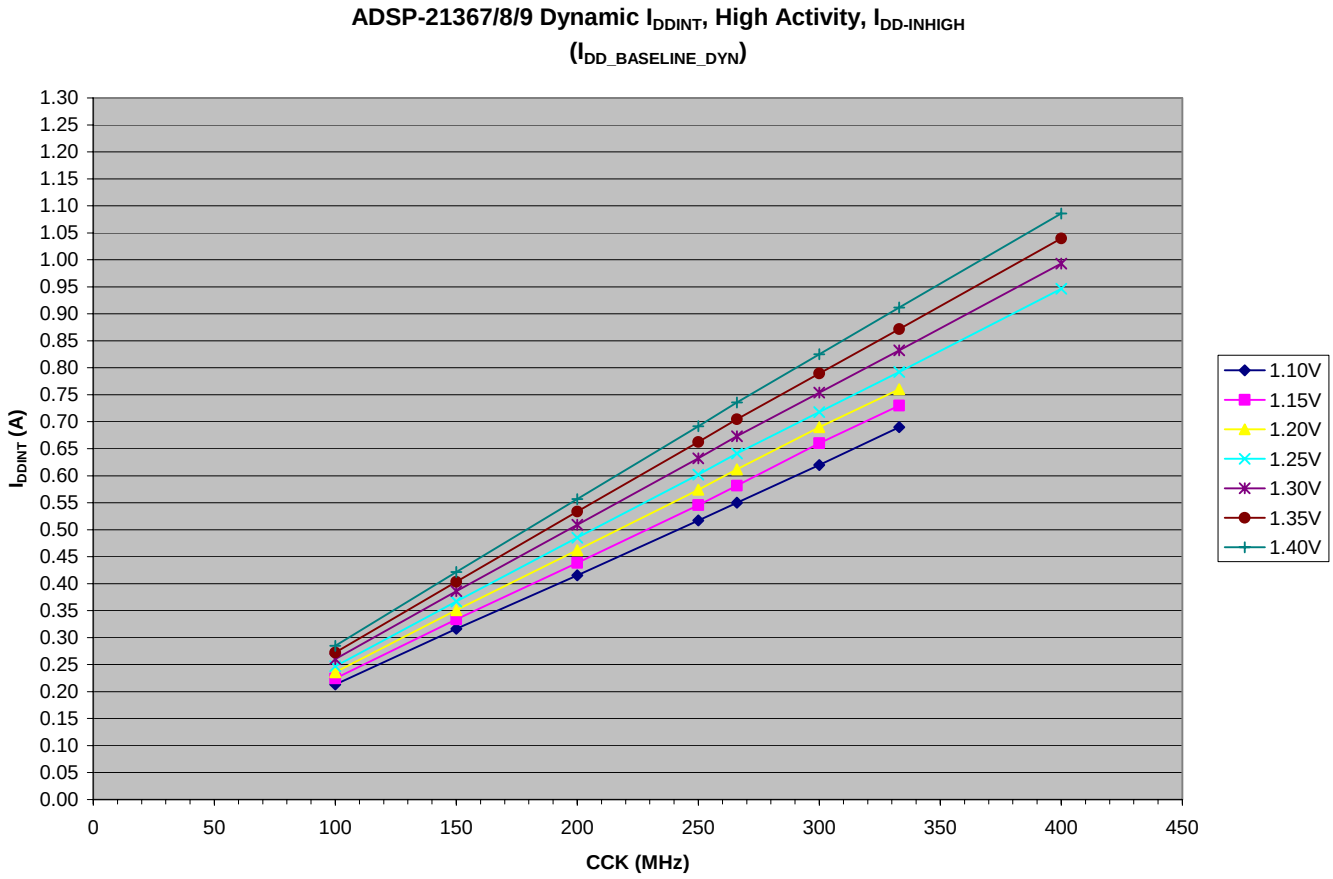

Figure 4. $I_{DD_BASELINE_DYN}$ graph

The ADSP-21368 processor is *not* specified for operation at 1.10 V or 1.40 V (V_{DDINT}). This curve is for reference only.

Appendix B

The ADSP-21367 and ADSP-21369 $I_{DD\text{-}STATIC}$ current graph for MQFP and LQFP 266 MHz and 333 MHz speed grade models is shown in Figure 5 (there is no ADSP-21368 version of the QFP package). The static current on the V_{DDINT} power supply domain is a function of temperature and voltage and is *not* a function of frequency or activity level. Each curve in the graph represents a baseline I_{DDINT} static current for a specified power supply measured at various junction temperatures (T_J). The $I_{DD\text{-}STATIC}$ current graph (Figure 5) represents the worst-case static currents as measured across the wafer fabrication process for the ADSP-21367 and ADSP-21369 processors.

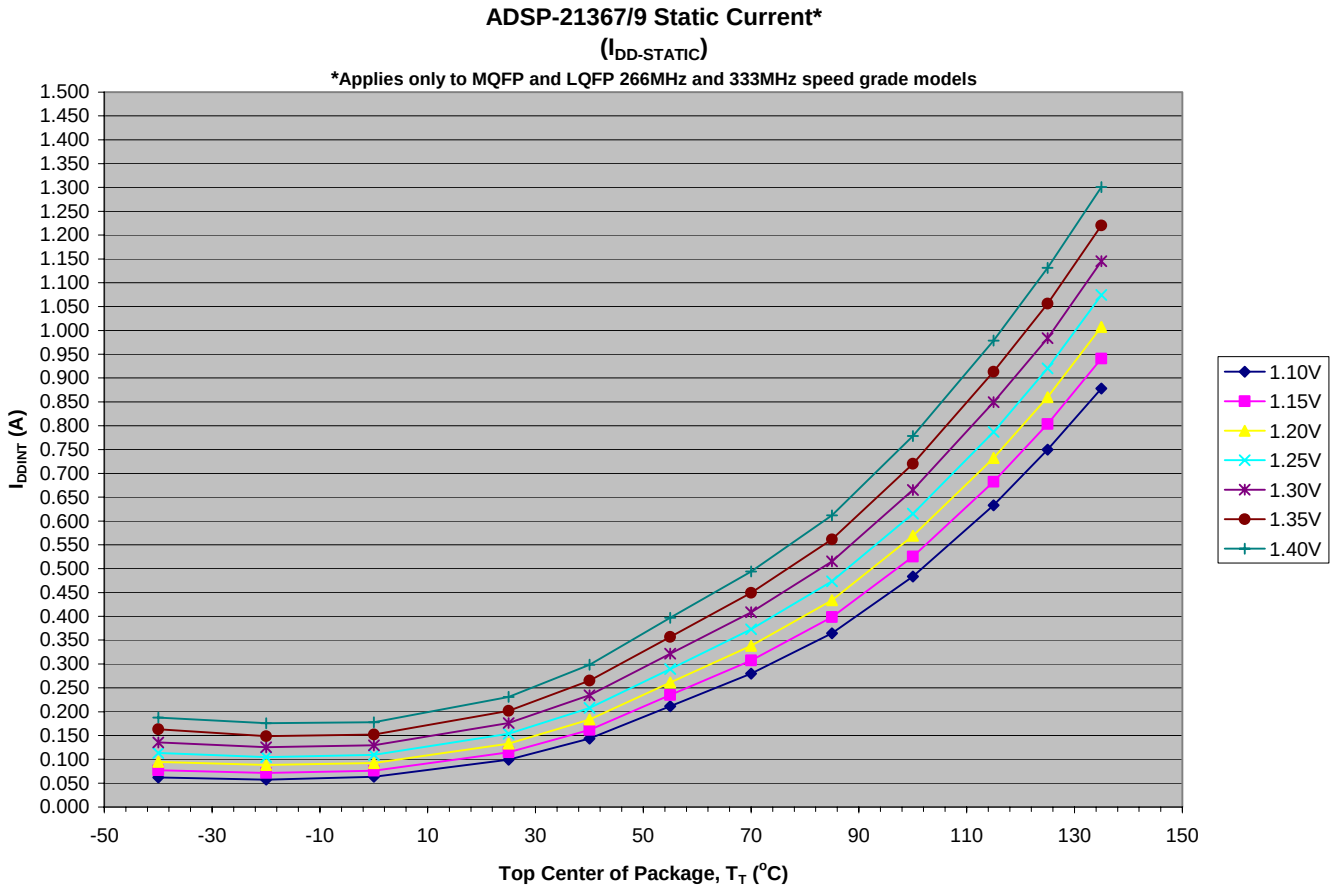

Figure 5. $I_{DD\text{-}STATIC}$ graph

The ADSP-21367 and ADSP-21369 processors are *not* specified for operation at 1.10 V or 1.40 V (V_{DDINT}). This curve is for reference only.

Appendix C

The ADSP-21368 $I_{DD\text{-}STATIC}$ current graph for Super BGA 333 MHz and 400 MHz speed grade models is shown in Figure 6. The static current on the V_{DDINT} power supply domain is a function of temperature and voltage and is *not* a function of frequency or activity level. Each curve in the graph represents a baseline I_{DDINT} static current for a specified power supply measured at various junction temperatures (T_J). The $I_{DD\text{-}STATIC}$ current graph (Figure 6) represents the worst-case static currents as measured across the wafer fabrication process for the ADSP-21368 processor.

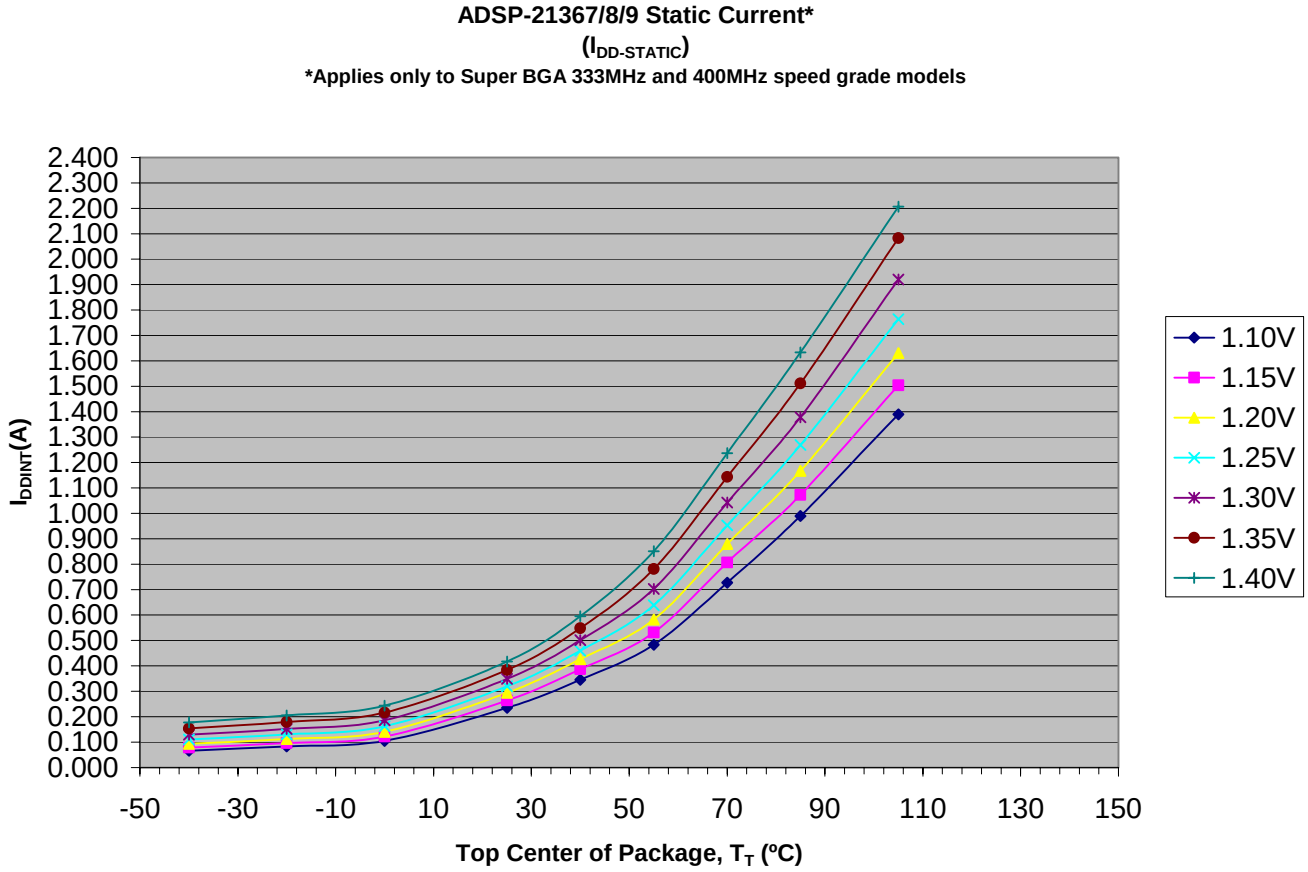

Figure 6 $I_{DD\text{-}STATIC}$ graph

The ADSP-21368 processor is *not* specified for operation at 1.10 V or 1.40 V (V_{DDINT}). This curve is for reference only.

Appendix D

Correct functional operation of the ADSP-21368 processor is guaranteed when the junction temperature of the device does not exceed the allowed junction temperature (T_J) as specified by the data sheet. For the ADSP-21368 processor, the total power budget is limited by the maximum allowed junction temperature (T_J) as specified by the data sheet.

The ABSOLUTE MAXIMUM RATINGS table in the ADSP-21368 data sheet states that exposure to junction temperatures greater than +125^{O}C for extended periods of time may affect device reliability.

To determine the junction temperature of the device while on the application printed circuit board (PCB), use the following equation found in the THERMAL CHARACTERISTICS section of the data sheet:

$$T_J = T_T + (P_{TOTAL} \, x \, \psi_{JT})$$

Equation 12 junction temperature (T_J) calculation

Where:

T_T = Package temperature (^{o}C) measured at the top center of the package

P_{TOTAL} = Total power consumption (Watts) as defined in Equation 10

ψ_{JT} = Junction-to-top (of package) characterization parameter (^{o}C/W)

Under natural convection, ψ_{JT} for a thin plastic package is relatively low. This means that under natural convection conditions, the junction temperature (T_J) is typically just a little higher than the temperature at the top-center of the package (T_T). The die is physically separated from the surface of the package by only a thin region of plastic mold compound. Unless the top of the package is forcibly cooled by significant airflow, there will be very little difference between T_T and T_J. However, note that ψ_{JT} is affected by airflow, and the values for ψ_{JT} under various airflow conditions are listed in the THERMAL CHARACTERISTICS section of the ADSP-21368 data sheet for the 256-ball sBGA, 208-lead MQFP and LQFP packages.

The THERMAL CHARACTERISTICS section of the data sheet also provides thermal resistance (θ_{JA}) values for the 256-ball Super BGA, 208-lead MQFP and LQFP packages. Data sheet values for θ_{JA} are provided for package comparison and PCB design considerations only and are not recommended for verifying T_J on an actual application PCB.

References

[1] *ADSP-21367/ADSP-21368/ADSP-21369 SHARC Processor Data Sheet*, Revision B, October 2007, Analog Devices, Inc.

[2] *ADSP-21368 SHARC Processor Hardware Reference*, Revision 1.0, September 2006. Analog Devices, Inc.

[3] *Estimating Power for the ADSP-21362 SHARC Processors (EE-277)*, Rev 1, January 2006. Analog Devices Inc.

Document History

Revision	Description
Rev 2 – February 11, 2008 *by John C.*	Added Super BGA 333-400 MHz Static IDD Graph.
Rev 1 – December 11, 2006 *by Chris C.*	Initial Release.